MAXIM Engineering Journal

Volume Thirty

News Briefs

MAXIM REPORTS RECORD REVENUES AND EARNINGS AND CONTINUED STRONG DEMAND FOR ITS PRODUCTS

Maxim Integrated Products, Inc., (MXIM) reported record net revenues of $135 million for the second quarter of fiscal 1998 ending December 27, 1997, compared to $104.7 million for the same quarter in fiscal 1997. Net income increased to $42.8 million in Q298 compared to $33.3 million for the second quarter of fiscal 1997. Diluted income per share was $0.29 per share for Q298 compared to $0.23 per share for the same period a year ago.

During the quarter, Maxim invested a total of $59.7 million in capital equipment, including the acquisition for $42 million of a sub-micron wafer fabrication facility in November 1997. The Company also purchased $55.1 million of its common stock during the quarter. Annualized return on average stockholders' equity for the quarter was 32%, one of the highest in the industry today.

During Q298, backlog shippable within the next 12 months increased to $208 million from the $182 million reported at the end of Q198. Eighty percent of the ending Q298 backlog consists of orders that were requested for shipment in Q398 or earlier. Customer inventories of Maxim products remained at low levels worldwide.

Net bookings in Q298 exceeded the record booking levels set in Q198. Although net bookings in the Pacific Rim were down slightly from Q198, they remained up from the levels recorded in Q3 and Q4 of fiscal 1997. Net bookings in Japan were lower in Q298 than in the previous four quarters. Net bookings in Europe and the United States were strong and exceeded Q198 levels.

Net bookings across the majority of the Company's product areas continued to be strong; however, the Company has seen significant weakness in orders from automatic test equipment customers, including several who primarily serve the Pacific Rim markets.

Gross margins for the second quarter increased slightly to 67% compared to 66.8% in Q198. Research and development expense increased by $1.5 million, to 12.6 % of net revenues. During the quarter, the Company also recorded a charge of $4.8 million to reduce the carrying value of certain pieces of capital equipment related to production, research and development, and administration.

Jack Gifford, Chairman, President and Chief Executive Officer, commented on the quarter: "We believe that the combination of record order rates and relatively low customer inventory levels suggests that end market consumption (demand) for the Company's products continues to be strong. Our broad product line, our new products targeted on emerging markets, and our geographically diverse business continue to serve Maxim well. Three-fourths of our net bookings during the quarter were derived from customers located in the United States and Europe."

Gifford continued: "Despite the economic issues affecting Pacific Rim companies, overall demand for our products is strong, reinforcing our belief that Maxim's ICs, and the value they offer, are critical to exports of electronic equipment by manufacturers worldwide."

MAXIM IS A FINALIST FOR 1997 INNOVATION OF THE YEAR AWARD

FINALIST

Maxim's MAX2102 has been named a finalist in *EDN* Magazine's 1997 Innovation of the Year competition. The MAX2102 is a direct-conversion tuner IC designed for digital direct-broadcast satellite applications. It directly tunes L-band signals to baseband using a broadband I/Q downconverter, thus eliminating expensive dual downconverter tuners in broadband systems.

EDN Magazine's Innovator and Innovation Awards are elected by *EDN* readers, who constitute an elite audience of design engineers.

Maxim also was honored by *Microwaves & RF* Magazine, which selected the MAX2102 as one of its "Top Products of 1997." Maxim received top billing in that competition.

New IC caps two decades of UART development

Maxim has introduced a tiny universal asynchronous receiver/transmitter (UART) that is compatible with the miniature electronic components in today's portable products. Compared with well-established UARTs already on the market, the new MAX3100 offers numerous advantages: lower cost, higher speed (to 230kbaud), lower power and lower voltage operation (<3V), and special features that include IrDA timing for IR communications and a FIFO buffer to relieve the processing burden in small systems.

Although more than 40 UART devices are available today, they either fail to satisfy some requirements of today's applications, or they satisfy requirements only through unwelcome trade-offs in size, power, or speed.

Maxim has identified a need—and a market opportunity—for a newly designed UART that directly meets today's speed and power requirements and offers the latest special features, without unwieldy workarounds. Our efforts have resulted in a new UART, the MAX3100.

The reason that such an extensive inventory of UARTs still fails to meet every modern requirement lies in the incremental nature of UART development. In this article, we review the UART in terms of its major technical developments, market evolution, and current trends.

UARTs in PC applications systems

One of the first large-scale-integration (LSI) chips ever developed (predating the single-chip microprocessor by several years), the UART has been available since the early 1970s. Constantly refined rather than reinvented, it has shown little change over the years in its pin names, function names, or general mode of operation. Modern CMOS UARTs like the National Semiconductor 16550 and the Zilog 8630 are traceable to early classics like the Intel 8250 and Intersil 6402.

In 1981, an 8250 UART was included on the original IBM PC motherboard to provide communications with modems and serial printers. Along with BIOS support in the PC, this early usage established the 8250 architecture and feature set as a de facto standard for UARTs. The basic architecture was extended over the years. As faster modems and application software such as "Laplink" drove the need for higher data rates, the 8250 responded with improved bus timing and higher speed—first to 115kbaud, then to 230kbaud. The result was a direct, high-speed extension of the 8250: the 16450 UART.

Higher speeds, however, revealed weaknesses in the interrupt latency and the response time of software buffering within the PC. At 115kbaud, for instance, a byte is available every 100µs. With 20µs of interrupt latency and a 30µs buffering time, this baud rate usurps 50% of a PC's CPU bandwidth. Such performance was clearly unacceptable for large applications running under a sluggish, non-real-time, windowed operating system.

The next extension in UART capability was to alleviate this overhead by including hardware buffering in the UART itself. Adding an 8-word FIFO to the basic 8250 produced the 16550 UART. Later incarnations increased the FIFO to 32 bytes (16C650) and 64 bytes (16C750). Larger FIFOs, however, share with cache memory the characteristic of diminishing returns vs. size. The next step in UART development would therefore appear to be a smart communications coprocessor, and such devices have just begun to emerge as add-on PC cards.

Because of cost pressures and the availability of VLSI in the late 1980s, the PC UART was pulled into a bit of VLSI called a "super I/O." This chip included two UARTs, a parallel printer port, a floppy port, and other devices associated with the I/O of a standard PC. The internal UARTs are recognizable as 16550s with compatible register sets and a lineage tracing back to the original PC and the 8250 UART.

The latest crop of super I/Os has further extended the architecture to include IrDA timing modes for IR serial communications. IrDA (Infrared Data Association) started life as a feature of palmtop computers, but is now employed to provide a simple noncable interface for printers and pay telephones. Other performance extensions include a boost to speeds of 460kbaud and even 920kbaud. The next step in PC UART technology should be interesting. Universal serial buses (USBs) and other higher speed interfaces are emerging, but the standard UART with RS-232 interface is not likely to vanish from PCs in the foreseeable future.

UARTs in large industrial systems

The PC, with its mainstream market penetration and consequent large-volume manufacturing, has clearly driven the development of UARTs. Non-PC systems are driven by the PC as well, because the host for most such

systems is a PC. Non-PC-system communications therefore require a UART compatible with the PC in speed and features. But non-PC applications are often constrained by power, size, or cost limitations, leading Maxim to observe that this market was not well served by the UARTs currently available.

Among the numerous ICs available for telecommunications, large industrial installations, and other large non-PC systems, the standard PC UART is most common. For these markets, the 8250 and Philips (Signetics) 2651 architectures have been extended to duals, quads, and (recently) even octals. The Zilog 8630 is strong in this market, thanks to its ability (several years ago) to run much faster than the 8250 of that time. The high-end 683XX microcontrollers (µCs) from Motorola also have a piece of the market. They typically include a 68000 core with various peripheral functions, and some are very flexible in executing complex communication tasks.

Today there is also a trend to include the UART function in custom ICs. As a relatively common, synthesizable logic function available as a Verilog or VHDL "megacell," the UART can be implemented in silicon along with other system functions, using modern EDA tools. This "system on a chip" model is gathering support as a solution for large digital systems, thanks to the availability of good tools and low-cost foundry services.

UARTs in small industrial systems

Modems, small industrial networks, and other small non-PC equipment require UARTs for communication with the ubiquitous PC. As a result, full-featured microcontrollers like the 80186, 8051, 68HC11, and Z8 have included UARTs since the early 1980s. This internal UART function has generally filled the need for low- to medium-speed communications in these applications. With a few notable exceptions, the speed and feature set of µC UARTs have remained relatively static over the years as µC manufacturers have pushed their products' clock speed, ROM size, and other features.

Exceptions include members of the Dallas Semiconductor 80C320 family of high-speed 8051 derivatives, which include two UARTs per chip. Members of the Intel 80C51FA family of full-featured 8051 derivatives include an enhanced UART that provides features for 9-bit network addressing (described later).

For applications in which high performance or an additional UART was required, the small-system designer historically had only two choices. If a simple, low-performance UART was acceptable and the system ROM size and bandwidth permitted, a UART could be implemented in software. (The many trade-offs involved in this decision are discussed later.) Otherwise, the designer added an external UART in most applications.

The external UART was usually a large (28 pins or more), full-featured device like the 8250. It was costly, required a lot of power and PC-board real estate, and usually exceeded the needs of the application. More importantly, it demanded an unwelcome level of software complexity to program around the unneeded features and implement the minimal features actually required.

To provide an advanced feature like 115kbaud IrDA support, the designer was obliged to implement an IrDA timing generator in a PAL and feed its output to a standard UART, usually external to the µC. IrDA timing chips have since emerged to replace the PAL, but the external UART is still required in most cases.

The smallest and lowest power systems (hand-held industrial equipment, bar-code readers, test equipment, and consumer products) often require very small µCs, and the lowest cost, lowest power µCs (the Microchip PIC 16C54 or Motorola 68HC05J2, for instance) do not include a UART. The solution for these systems is usually a software UART, in which the serial-communications function (when active) absorbs a large portion of the CPU bandwidth.

If a better UART was required for reasons of bandwidth or performance, the designer usually turned to a higher end µC with the UART included. If the application required features not supported by this minimal UART function, the designer was obliged to use a large, full-featured UART. Either way, the design was untenable. The designer could develop a custom UART if the manufacturing volumes permitted. If not, the desired feature had to be compromised or eliminated.

DSPs are another class of applications poorly served by modern UARTs. Many DSPs (like the TMS320C10 from Texas Instruments) do not include a UART. Many DSP applications implement the UART in software, but that approach is especially problematic in a DSP system. Such systems generally run large synchronous programs that have difficulty responding to serial traffic and other asynchronous inputs.

The need for a small, modern UART

Maxim perceived the market need and product opportunity in a new UART that would meet the non-PC requirements outlined above. Although UARTs are primarily digital and Maxim is primarily an analog/mixed-signal

company, Maxim has gained extensive serial-interface experience through the development of single-supply interface ICs like the MAX232 and MAX485. Maxim saw the need for a UART that:

- Supports high speed
- Supports low-voltage (<3V) and low-power operation
- Fits in a very small package, with baud-rate generator and all other support circuitry on board
- Includes zero-power shutdown and wake-up on received signal
- Supports IrDA communications timing
- Includes FIFO receive buffer to alleviate communications overhead in small processors
- Includes Schmitt-trigger inputs and high output drive, for direct optocoupler interface in isolated systems
- Remains cost competitive

In converting these requirements to silicon, Maxim has produced a tiny, full-featured UART called the MAX3100 (described later). To help minimize size and pin count, it features a synchronous serial peripheral interface (SPI) for communications. A serial interface for a serial-interface IC may sound paradoxical, but it enables a complete, full-featured UART to fit in the footprint of an SO-8 package (the actual package is a 16-pin QSOP).

Many µCs include the serial interface built into the MAX3100. For those that don't, a "bit-banged" serial interface can easily be implemented. Thus, the MAX3100 enables high-performance communications for most systems—without major trade-offs in size, cost, and power, and without the additional trade-offs associated with a software UART.

Software-based UART trade-offs

For µCs that lack an internal UART, the simple and seemingly obvious way to implement serial communications is through software. Extra hardware is not required, and the µC then handles its own communications. The designer can indeed eliminate a hardware UART by creating one in software, but that arrangement has its own problems and costs. Except in the simplest cases, the true cost of a software UART must include the percentage of computational time demanded from the CPU. Realistically, a software UART is more costly than a hardware UART.

Software UARTs require substantial resources. In most cases a counter/timer (crucial in µCs) is needed to generate time slices for the serial bit cells. At least two I/O ports are required for the serial input and output (RX and TX), and RX should have an interrupt capability that allows incoming start bits to synchronize the incoming data (**Figure 1)**. If handshaking is required (via the CTS and RTS terminals, for example), the system may require other port pins as well. Because reliable reception requires that the maximum interrupt latency be kept well below one-half of a bit interval, the interrupt requirement complicates system designs **(Figure 2)**. Small microprocessors (µPs) can be overwhelmed, especially at high baud rates **(Figure 3)**.

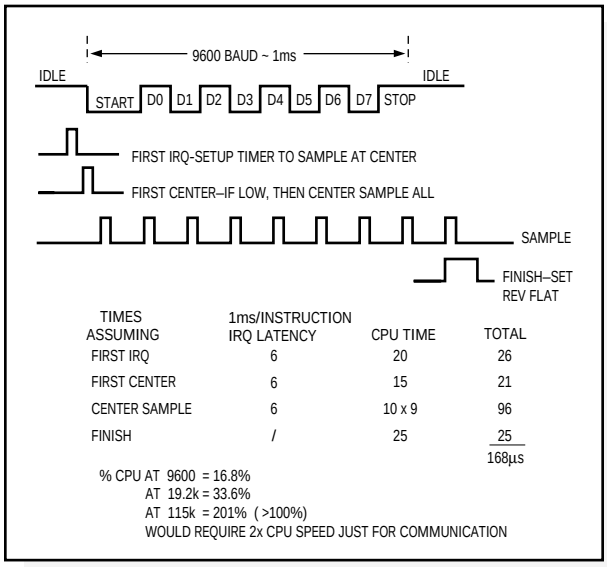


Figure 1. Software UARTs place a heavy computational load on the CPU.

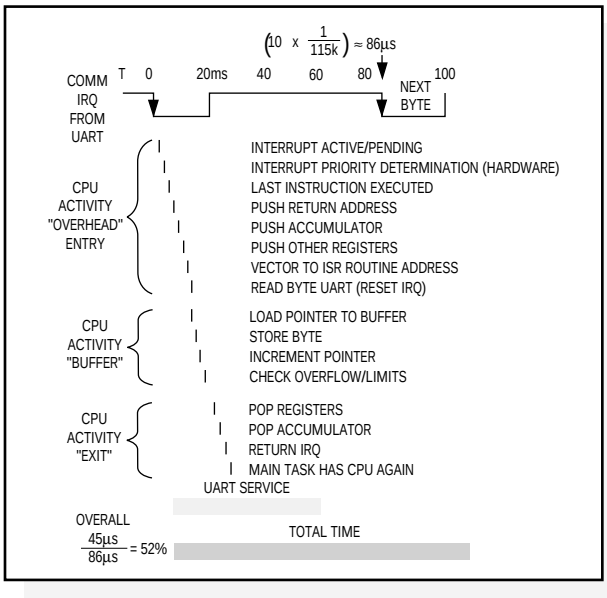


Figure 2. These details show how the CPU time is allotted in servicing a software UART.

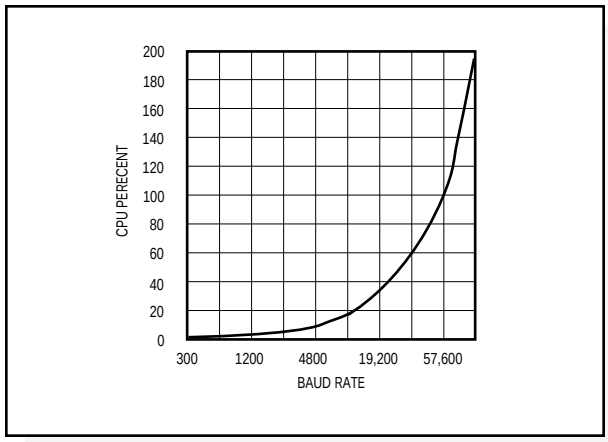


Figure 3. The percentage of CPU time required for servicing a software UART rises sharply with the baud rate.

A software UART generally requires 200 to 500 bytes of code, depending on its sophistication and the µP's capability. This requirement makes the software-UART option unworkable for many of the smaller µCs, whose total code space might be only 500 bytes. Finally, a software UART's power drain can be significant. Wake-up time for the µC is greater than a baud period in most cases, so to be ready for possible serial traffic it must run continuously.

In contrast, a MAX3100 UART system offers numerous advantages: it implements a full handshaking interface with only four port lines. A fifth line (an interrupt line) is optional. Code size is about 50 bytes. The µP/UART combination can save a tremendous amount of power by going into sleep mode between serial-data transmissions. Finally, the MAX3100's timing requirements do not change with the baud rate. Its internal FIFO stack alleviates much of the real-time processing burden caused by the burst-mode message traffic common in small systems.

MAX3100 description

The MAX3100 UART provides an interface between the synchronous serial-data port of a µP (compatible with SPI™, QSPI™, and Microwire™ standards), and an asynchronous serial-data communications port such as RS-232, RS-485, or IrDA. For a brief description of SPI, see the sidebar to this article, "Serial Peripheral Interfaces."

The MAX3100 combines a simple UART and baud-rate generator with an SPI interface and interrupt generator. Writing to an internal register configures the UART for baud rate, data-word length, parity enable, and enable of the 8-word receive FIFO. This "write configuration" register contains four interrupt-mask bits, and it also selects between normal UART and IrDA timing.

The programmable baud-rate generator is capable of rates from 300baud to 230kbaud **(Figure 4)**. Bits B0–B3 in the write-configuration register determine the baud-rate divisor (BRD), which divides down the frequency of the crystal between terminals X1 and X2. The MAX3100 oscillator accepts a crystal of 1.8432MHz or 3.6864MHz, and it also accepts a square wave at X1 with a 45% to 55% duty cycle.

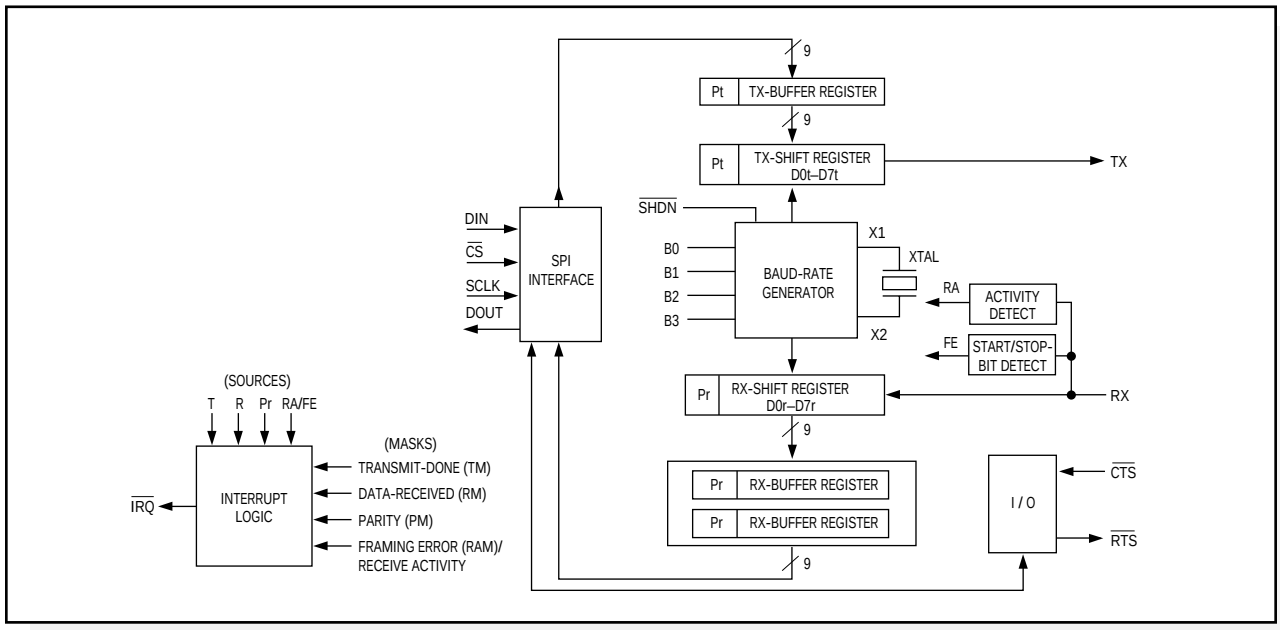


Figure 4. A new version of the venerable UART enables 8051 microcontrollers to communicate using an IrDA data link.

SPI and QSPI are trademarks of Motorola, Inc. Microwire and Microwire Plus are trademarks of National Semiconductor Corp.

The transmitter section accepts SPI/Microwire data, formats and loads it into the transmitter buffer register, and shifts it in asynchronous-serial format to the TX output. Internal logic adds start and stop bits and clocks the data out at the selected baud rate. The receiver section accepts data in serial form and detects the start bit on a high-to-low transition. The center of this start bit is defined by a majority vote (minimum 2 of 3) following the 7th, 8th, and 9th samples of the internal 16x baud clock **(Figure 5)**. An 8-word FIFO stores the received data. At the center of the first stop bit, the receiver begins searching for the next start bit.

Opto-conditioned inputs and outputs enable the MAX3100 to receive optocoupler outputs and drive optocoupler inputs directly. That is, the UART's receiver input (RX) is a Schmitt-trigger circuit, and its transmitter output (TX) is capable of sinking 25mA. The MAX3100 also includes two general-purpose ports with opto-conditioning ($\overline{RTS}$ and $\overline{CTS}$), which are useful for handshaking and control (RS-232 and RS-485 driver enable, respectively).

The MAX3100's 8-word FIFO and interrupt logic conserves CPU computing time. By allowing up to eight characters to be read each time, the CPU services a receive-activity interrupt (RA), and the FIFO buffers the CPU transfer rate from the UART's serial-data rate. The MAX3100's one interrupt input can be set by any of four sources: parity received (Pr), received data (R), receiver activity/framing error (RA/FE), and transmit buffer empty (T). Any or all sources can be masked.

As an additional feature of this SPI UART, the MAX3100 offers an IrDA timing mode suitable for communication with other serial infrared (SIR)-compatible devices, or for reducing power in opto-isolated applications **(Figure 6)**. The MAX3100 was designed to drive opto-isolators directly, so to drive a serial-IR module like the HP HDSL-1000 the logic must be reversed. In IrDA mode, a bit period is shortened to 3/16 of a baud period (1.6µs at 115kbaud). With TX at logic low and RX at logic high, a data zero is transmitted as a negative pulse.

In receive mode, the MAX3100 samples an RX signal halfway into a high-level transmission. This sampling occurs once, rather than three times as in the normal mode. The MAX3100 ignores pulses shorter than 1/16 (approximately) of a baud period, and the IrDA device communicating with the MAX3100 must be set to transmit pulses at 3/16 of the baud period.

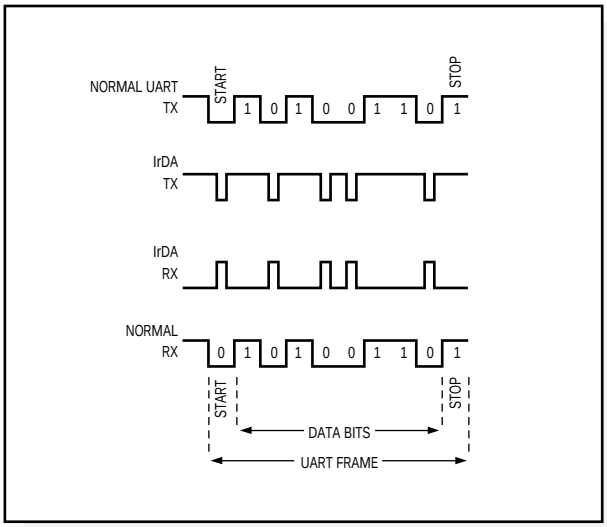


Figure 6. The narrow pulses used in IrDA communications consume less power.

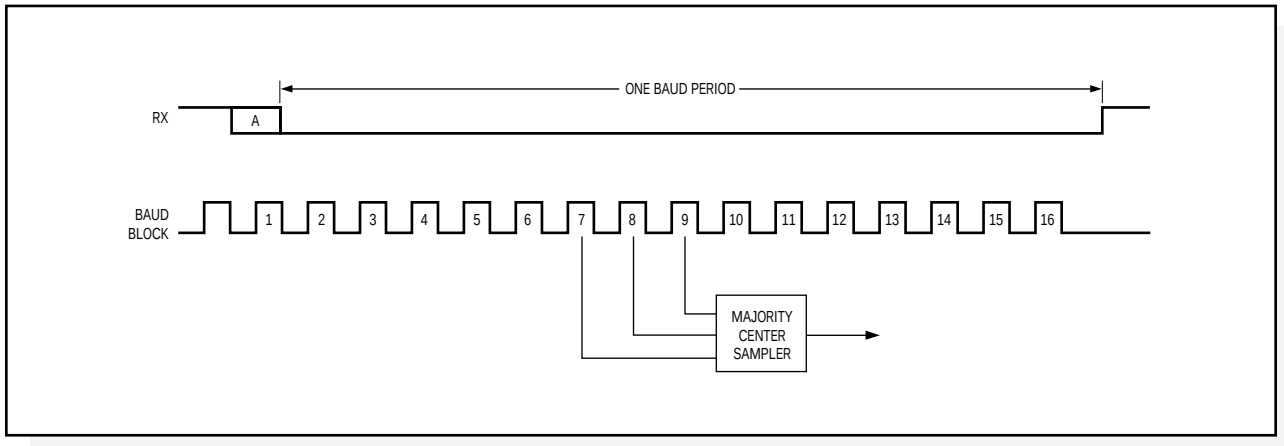


Figure 5. The MAX3100 identifies an incoming start bit if at least two of the three mid-pulse samples are low.

The MAX3100 enables new applications

The circuit of **Figure 7** enables any derivative of the 8051 µC to communicate using the serial-infrared (SIR) format established by IrDA. Communication is a two-stage process in which the µC first transmits via a "bit-banged" SPI serial interface to the MAX3100 (IC1), and IC1 in turn formats the message in IrDA mode. The UART in many 8051 derivatives is not IrDA compatible, and cannot easily be made so. The circuit shown, however, provides the communication link and is easily added to an existing 8051 system with a minimum of cost, power, and software code.

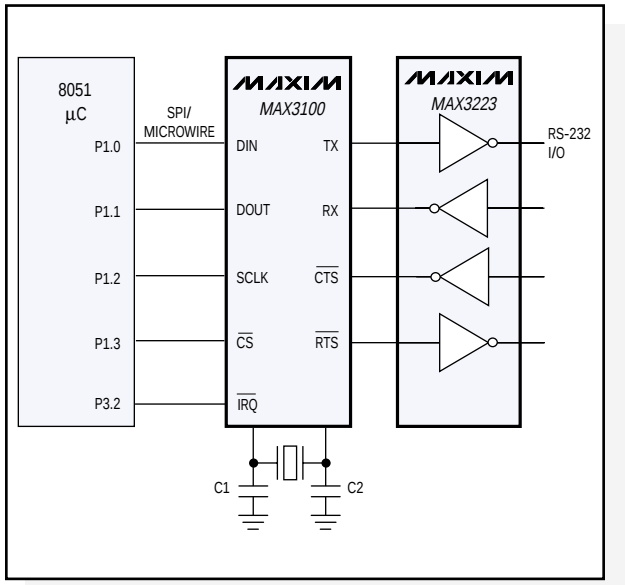


Figure 7. The MAX3100 enables IrDA communications by variants of the 8051 microcontroller.

The MAX3100 is capable of 115kbaud, but in this case the optical components shown limit the data rate to 4800 baud. The components are inexpensive, however, and most IrDA devices support data rates as low as 2400 baud. If necessary, the maximum 115kbaud is easily achieved with higher-quality optical components such as the HP-1000 IrDA module. Most IR LEDs and photodiodes are acceptable for this application, but to avoid being swamped by visible light the photodiode should include a filter. If necessary, place an external ambient-light filter in front of an unfiltered photodiode.

The operating voltage can range from 2.7V to 6V, subject to limitations imposed by the 8051. Power-supply current is about 1mA for IC1 plus 1mA per megahertz for most variants of the 8051. Timing for the SPI interface is not critical. The UART performs all real-time processing, so the processor clock can have any reasonable frequency. Unlike most system clocks, this one does not require time and temperature stability.

The MAX3100-8051 driver code is available at Maxim's website (www.maxim-ic.com). See "IrDA code for MAX3100 UART-8051" under the heading *Other Software*. In the MAX3100-8051 driver code the subroutine UTLK provides driver support for the MAX3100. This code translates from IrDA to RS-232 and back (for demonstration and test purposes), using the 8051's internal UART to talk on the RS-232 side. See code for details.

There are other alternatives but they carry drawbacks. One such alternative is to write a software routine for IrDA UARTs at low data rates, but the software is tricky. It uses up to 100% of the CPU's attention when active, and is impractical above 2400baud. IrDA timing can also be generated with discrete logic or a PAL, but that approach is expensive, power-hungry, and requires an external baud generator for the clock source.

9-bit networks

The MAX3100 supports a common multidrop communication technique known as 9-bit mode **(Figure 8)**. It uses the parity bit to indicate a message that contains a header with destination address. The MAX3100 parity mask can be set to generate interrupts for this condition. Operating a network in 9-bit mode lowers the processor overhead at all nodes by enabling the slave controllers to ignore most of the message traffic. The remote processor is then free to handle more useful tasks.

Nine-bit mode configures the MAX3100 for eight bits plus a parity bit, which is cleared for normal messages and set for address-type messages. Parity-interrupt masks at the MAX3100 nodes are set to generate an interrupt at high parity. The result is that standard messages are ignored because they have a cleared parity bit, and each address-type message triggers an interrupt that causes it to be captured and examined by all MAX3100s. The MAX3100 for which the message is intended processes the remainder of the message, while all others ignore it.

Because the 9th-bit parity interrupt is controlled by data in the receive register and not by data in the FIFO, it is most effective with the FIFO disabled. With the FIFO disabled, the received nonaddress words can be ignored and not even read from the UART.

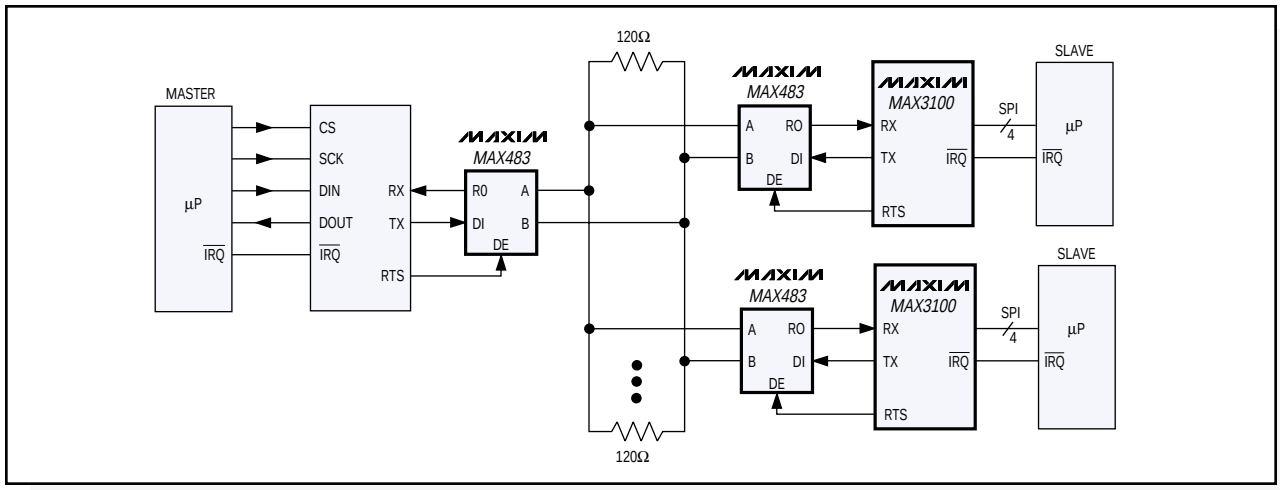


Figure 8. Nine-bit networks reduce the processing overhead in a communication network.

In an isolated serial interface **(Figure 9)**, the MAX3100 Schmitt-trigger inputs are driven directly by the optocoupler outputs. The optocoupler's skew does not affect timing at the asynchronous serial output, so only the SPI interface setup and hold times must be met. On the asynchronous side, you can create a bidirectional, opto-isolated interface using only two opto-isolators (one each for RX and TX). In that case, the narrow baud periods (3/16 wide) used in IrDA communications provide a power savings of 81%.

A separate discussion on serial peripheral interfaces begins on page 10.

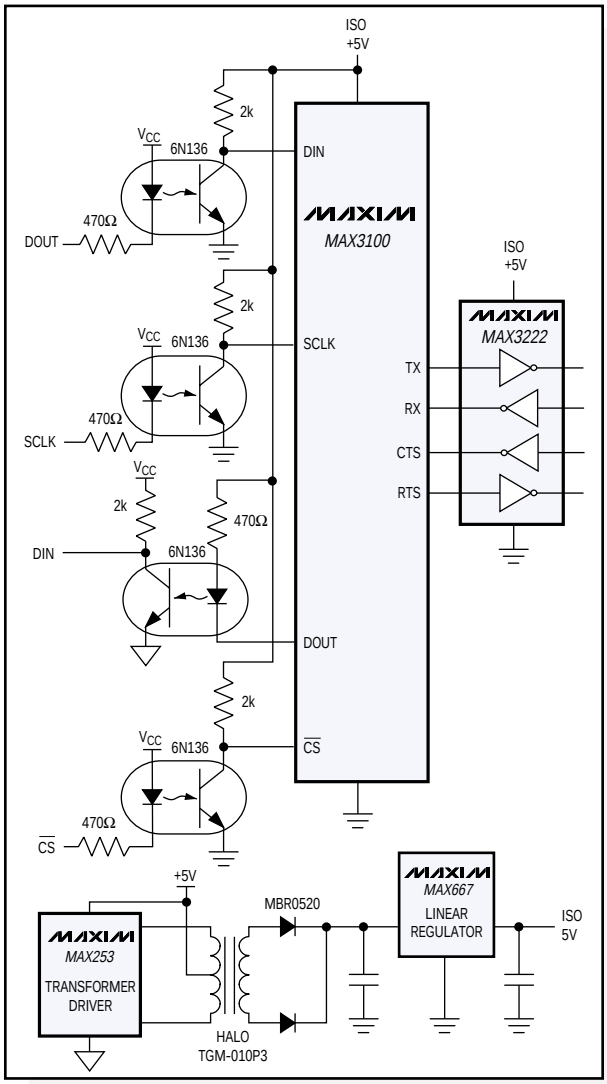


Figure 9. MAX3100 I/O pins are designed for a direct interface to optocouplers.

Serial peripheral interfaces

As a serially accessed peripheral, the MAX3100 has the minimal number of package pins. Its synchronous-serial interface is compatible with the SPI™ and QSPI™ standards from Motorola and the Microwire™ standard from National Semiconductor. For systems in which the µC contains no hardware support, these simple interfaces can easily be implemented in a few lines of code. For the following protocol families, note that the maximum clock rates mentioned are subject to further limitation in a given application.

Microwire and Microwire Plus

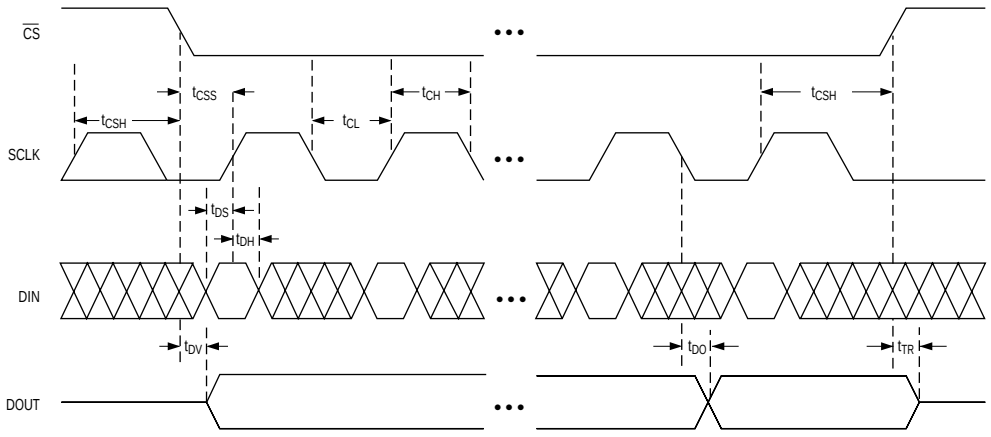
As a 4-wire serial interface used on COP controllers from National Semiconductor, Microwire includes clock, data-in, data-out, and chip-select lines. Its maximum clock rate is 250kHz, with a corresponding minimum "high" interval of 1µs.

Although Microwire peripherals accommodate digital words of arbitrary bit length, they usually operate on 16-bit words. Data into the device should be valid on the clock's rising edge, and data out of the device is synchronized with the clock's falling edge. Chip selects have a nonstandard, active-high polarity. Microwire Plus, which is used on National Semiconductor's HPC series of controllers, reverses the clock phase for data in and data out, and also speeds up the interface timing.

SPI and QSPI

The SPI interface used on Motorola's line of controllers is very similar to National Semiconductor's Microwire. Though restricted to 8-bit-multiple digital words, it also consists of a clock line, data-in and data-out lines, and a chip-select line (see figure). The maximum clock rate is higher than that of Microwire: 1Mbps to 2Mbps (depending on the processor) for SPI, and more than 10Mbps for QSPI.

QSPI and SPI are indistinguishable to an external slave device. QSPI automates the SPI process with an automatic chip-select generator and a 16-level hardware queue internal to the controller. QSPI also gives digital control over the clocking of data in and out: a CPHA bit controls the clocking phase and a CPOL bit controls the marking polarity.



This SPI serial-interface timing is closely related to that of the QSPI and Microwire standards.

Tiny analog switch alleviates I²C address conflicts

To avoid address conflicts, every peripheral on an I²C™ bus must have a unique address. Sometimes, however, peripherals may be assigned the same address. The circuit of **Figure 1** resolves address conflicts by enabling the I²C bus to select between two peripherals with the same address.

The popular I²C bus is an open-collector, 2-wire interface that includes a clock line and a bidirectional data line. It allows a controller (the master) to select a particular device (the slave) by first issuing a serial address on the data line, then issuing appropriate commands or data. Master and slave can send data in both directions by pulling the data line low, and slaves can generate wait states by pulling the clock line low. Bus switching, however, is complicated by the open-collector architecture—it cannot be accomplished with the CMOS outputs of AND gates or 74HC157 data selectors.

The peripherals shown in **Figure 1** are a Philips I²C real-time clock (PCF-8583) and a large I²C EEPROM (Microchip M-24LC16). Both have an internal, hexadecimal slave address of A0. (The EEPROM takes up the entire address range, making it impossible to avoid.) The analog switch connects either one device or the other. Selection involves the data line (SDA) only, because an I²C start condition requires that the SDA signal goes low before the clock goes low. To select between the devices, the master device sets a port pin to control the state of the dual SPST analog switch.

IC1 is a CMOS chip well suited to this function. Its normally open switch and normally closed switch perform the 2:1 selector operation with no additional inverters or port lines. It features low on-resistance (33Ω) and low supply current (1µA), and is specified for operation below 3V. Also, its tiny 8-pin SOT package (µMAX) is only one-half the size of an SO-8 package.

A similar idea appeared in the 6/23/97 issue of Electronic Design.

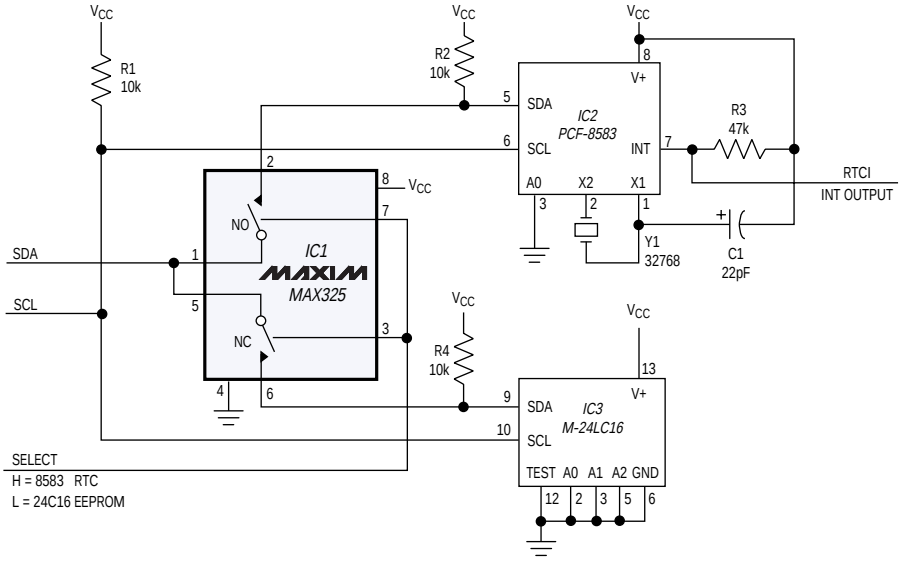


Figure 1. A dual analog switch (IC1) and a single controller line (SELECT) enable this I²C bus to select between two peripherals with identical addresses.

I²C is a trademark of the Philips Corporation.

Transformer-driver IC controls bidirectional switch

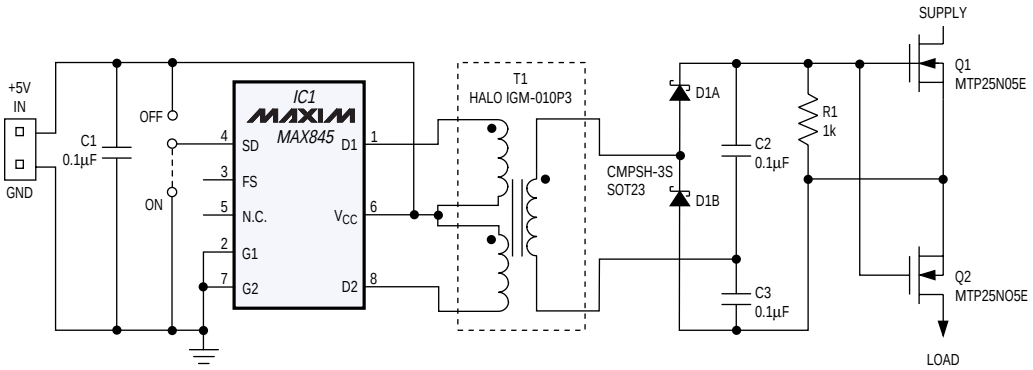


Figure 1. This bidirectional power switch handles moderately high positive, negative, and AC supply voltages.

The circuit of **Figure 1** is simply an on/off switch that connects V_{SUPPLY} to a load. V_{SUPPLY} can be positive, negative, or AC, with magnitude limited only by the MOSFETs' maximum V_{DS} rating. For the device shown, that limit is 50V.

The transformer's primary winding and driver IC operate on 5V, generating an isolated secondary waveform that is rectified by D1 and D2 to produce a 10V V_{GS} for the n-channel MOSFETs. V_{GS} is isolated, constant, and unaffected by changes in V_{DS} with respect to ground. Because the combination of a single MOSFET and negative V_{GS} would allow current flow in the off state (due to forward bias on its internal parasitic diode), two MOSFETs are connected source-to-source. Their internal diodes are then opposed, blocking unwanted current flow of either polarity in the off state.

Shutting down the IC turns off the switch by removing V_{GS} from the MOSFETs (SD = 5V turns the switch off; SD = 0V turns it on). The speed of this turn-off depends on the value of R1; lower values reduce turn-off delay at the expense of higher supply current. (For R1 = 1kΩ, the supply current is 24mA.) If speed is not an issue, reduce the supply current to 5mA by substituting a larger R1. **Figure 2** shows this circuit operating with a 40V, 1.2A load.

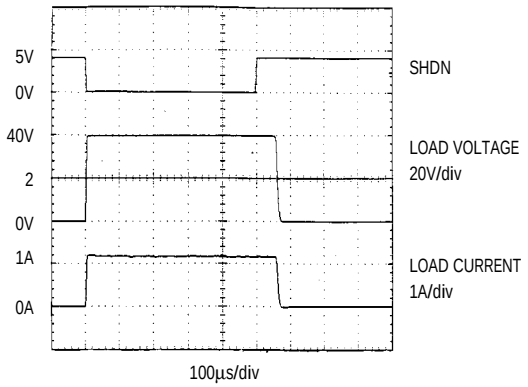


Figure 2. This scope plot shows the Figure 1 circuit operating with a 40V, 1.2A load.

Other switching techniques have drawbacks. Relays, for instance, have switch bounce and high power consumption (about 0.5W). The maximum V_{GS} rating for most power MOSFETs (approximately 20V for standard devices, 15V for logic-level devices) makes it difficult to withstand voltages greater than 15V. It can be accomplished by level-shifting the gate voltage, but that approach wastes power. In addition, the larger gate resistor required for higher voltages slows the switching speed.

A similar idea appeared in the 7/17/97 issue of EDN.

IR sensor/monitor wakes host system

The sensor/monitor circuit of **Figure 1** "wakes up" the host system on detection of infrared (IR) signals. It draws so little supply current that it can remain continuously on in a notebook computer or PDA device. Its ultra-low current drain (4µA maximum, 2.5µA typical) is primarily that of the comparator/reference device IC1.

The circuit is intended for the noncarrier systems common in Infrared Data Association (IrDA) applications. It also operates with carrier protocols such as those of TV remote controllers and Newton/Sharp ASK (an Amplitude Shift Keying protocol developed by Sharp and used in the Apple Newton). The range for 115,000-baud IrDA is limited to about 6 inches, but for 2400-baud IrDA it improves to more than 1 foot.

Immunity to ambient light is very good, although bright flashes usually cause false triggers. To handle occasional false triggers, the system simply looks for IR activity after waking and then returns to sleep mode if none is present.

The sensor shown (D1), a relatively large-area photodiode packaged in an IR-filter material, produces about 60µA when exposed to heavy illumination (and 0.4V when open-circuited). Most such photodiodes are acceptable in this circuit. Operation is in the photovoltaic mode (without applied bias). This mode is slow and not generally used in photodiode circuits, but speed is not essential here. The photovoltaic mode simplifies the circuit and saves a significant amount of power. In a more conventional configuration (i.e., photoconductive), photo currents caused by ambient light and sourced by the bias network would increase the quiescent current approximately ten times.

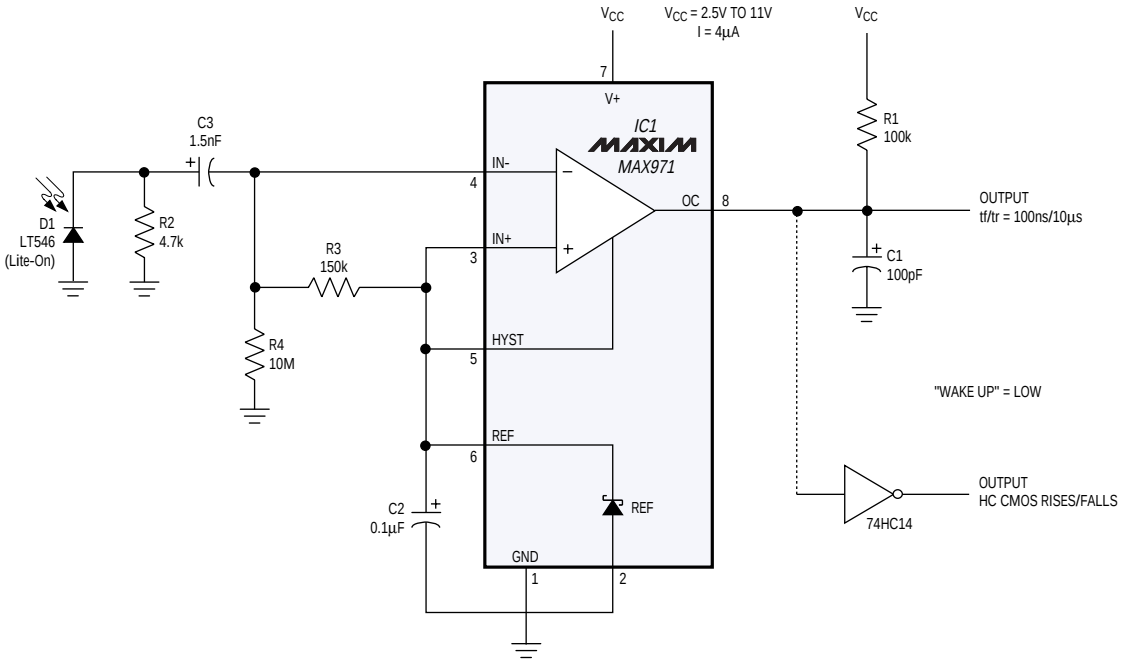


Figure 1. This low-quiescent-current circuit (4µA maximum) interrupts the host processor when it detects an IR signal.

V_{REF} and the R3/R4 divider introduce an 18mV bias between the comparator inputs. Derived from the reference, this bias is independent of the supply voltage. To suppress 60Hz/120Hz hum and other low-frequency disturbances, C3 and the R3/R4 divider form a highpass network with a cutoff frequency of 700Hz. C3 is normally charged to V_{REF} minus the 18mV bias, and any voltage produced by photocurrent through R2 adds to the voltage on C3.

Thus, any IR signal across R2 that exceeds the 18mV threshold trips the comparator and causes its output to go low (18mV represents a good tradeoff between range, noise immunity, and DC stability.) The low value of R2 prevents saturation of the photodiode in ambient light. If saturation is an issue, the R2 value can be reduced further—with a penalty in sensitivity and a boost in speed.

The comparator's input offset voltage (10mV maximum) sets worst-case extremes of 6mV and 28mV for the IR trip threshold, but this spread is not a significant issue. Typical spreads are much smaller than the maximums, and typical IR signals generate more than 60mV. A variation in offset affects the amount of overdrive, and therefore affects only the comparator's response speed.

The circuit's output can trip a set-reset flip-flop or interrupt a sleeping processor. The optional HCMOS gate (preferably a Schmitt-trigger type) can improve the output rise/fall times with very little effect on the overall quiescent current.

A similar idea appeared in the 10/13/97 issue of Electronic Design.

Small photodiode receiver handles fiber optic data rates to 800kbps

Combining a photodiode with two op amps and a comparator **(Figure 1)** forms a fiber optic receiver capable of data rates to 800kbps. Small packages (5-pin SOT23 for the op amps, 8-pin µMAX for the comparator) minimize the required real estate on a PC board or hybrid substrate.

The photodiode operates in the photoconductive mode, producing a signal voltage at IC1 whose transimpedance gain is equal to the value of R1 (4700Ω, in this case). The op amps (IC1 and IC2) are configured as noninverting amplifiers with gains of approximately 25V/V each, so the circuit's overall transimpedance gain is just under 3MΩ: 4700Ω x 25 x 25 = 2.99MΩ. The op amps' gain-bandwidth capability sets the maximum practical data rate at 800kbps.

Capacitive coupling between IC1 and IC2 negates the amplification of IC1's offset voltage. To achieve an optimum signal amplitude and symmetry, the R6/R11 divider sets IC2's reference voltage at 2.5V. The R12/R13 divider, which sets the comparator's reference somewhat higher (2.6V), provides a noise margin for the system and ensures that the comparator output remains low during a "no signal" condition.

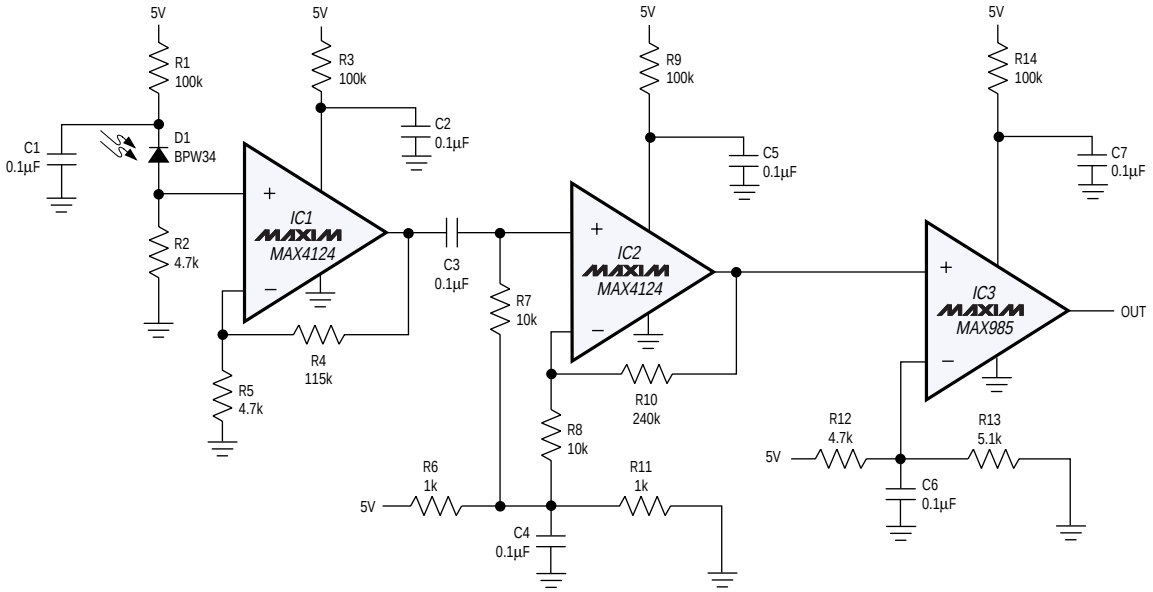


Figure 1. These two op amps and comparator form a tiny photodiode receiver for data rates to 800kbps.

Capacitive coupling cannot maintain a DC signal; instead, it allows DC portions of the signal to "relax" toward the reference level as shown in **Figure 2.** This effect, particularly noticeable for signals that appear after a long quiet period, is directly affected by the R7C3 time constant. R7C3 should be as large as possible to minimize the relaxation effect, but R7 should remain approximately 10kΩ (to minimize offset voltage by matching the inverting-input source resistance). The comparator cannot switch when its input is below the reference level, so too much relaxation can cause a loss of data at the end of a long string of 1s or 0s **(Figure 3)**.

Again, the IC3 reference should be slightly higher than the IC2 reference for a logic-low no-signal output (otherwise, set the IC3 reference lower). This ΔV_{REF} provides a system noise margin that can be adjusted via the R12/R13 divider, but be aware of the tradeoff: ΔV_{REF} going too low allows erroneous output transitions, and going too high degrades timing of the received signal. Set ΔV_{REF} as low as possible without causing erroneous transitions, making allowance for the offset voltages in IC2 and IC3.

The system is designed for 5V operation, but with a minor degradation in data rate it can operate at 3.3V or even 3V. Reducing the supply voltage increases the photodiode's internal capacitance (inversely proportional to the applied bias voltage), which forms a lowpass pole with R2 that limits the photodiode's frequency response. To a lesser degree, the lower supply voltage also limits response by producing a smaller gain-bandwidth product in the amplifiers. The circuitry is designed to accommodate a change in supply voltage with only one adjustment: ΔV_{REF} changes with supply voltage, so the R12/R13 divider must be adjusted as required to re-establish the desired noise margin.

A similar idea appeared in the 10/1/97 issue of Electronic Design.

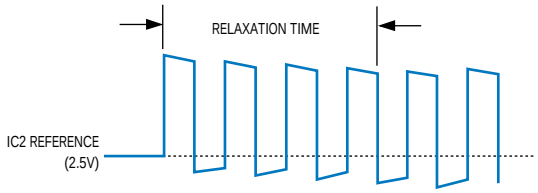


Figure 2. Figure 1's coupling capacitor (C3) causes a "signal relaxation" in the waveform at IC2's output and noninverting input.

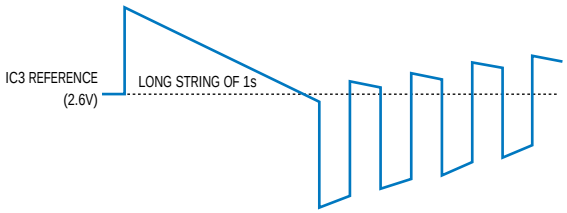


Figure 3. This waveform (from Figure 1's IC2 output) shows that signal relaxation can cause data loss. (The comparator output goes low when the waveform crosses its reference level.)

NEW PRODUCTS

First 2x4-channel, 14-bit ADCs to sample four channels simultaneously

The MAX125/MAX126 simultaneous-sampling ADCs perform power monitoring and 3-phase motor control. These 2x4-channel, 14-bit converters are the only such devices capable of simultaneously monitoring four channels at the 14-bit level, while preserving the sampled inputs' relative phase information.

These devices include four track/holds with a 2-channel multiplexer on each analog input, and each input is fault-protected to ±17V. An on-board programmable microsequencer enables the ADCs to convert from one to four channels. The maximum throughput rate when sampling all four channels is 75ksps per channel, and the conversion results are stored sequentially in the internal 4x14 RAM until accessed by the user.

The MAX125 accepts ±5V analog inputs; the MAX126 accepts ±2.5V inputs. Both feature an internal 2.5V reference, a low-power mode of operation, and a 14-bit parallel interface. They operate on ±5V supplies and are available in a 36-pin SSOP package. Prices start at $13.95 (1000 up, FOB USA).

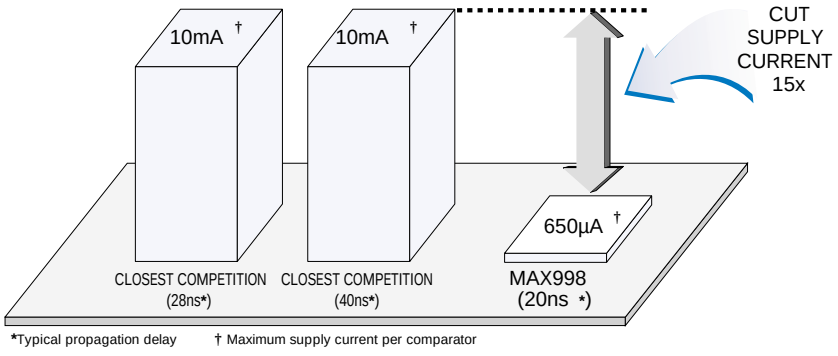
High-speed, low-power comparators are optimized for 3V/5V applications

The MAX998/MAX976/MAX978 single/dual/quad high-speed, low-power comparators are optimized for use in 3V or 5V single-supply applications. They draw supply currents of 300µA per comparator, achieve propagation delays of only 20ns (40ns max), and have the best speed/power ratio in the industry. The MAX998 has shutdown capability that places the output in a high-impedance state and reduces the supply current to 1nA.

All MAX998/MAX976/MAX978 inputs have a common-mode voltage range that extends 200mV below ground. The outputs, capable of Rail-to-Rail® operation without external pull-up circuitry, are ideal for use with TTL/CMOS logic. Inputs and outputs tolerate a continuous short circuit to either rail, and internal hysteresis ensures clean output switching, even for slow-moving input signals.

The MAX998 comes in a 6-pin SOT23 or 8-pin SO package. The MAX976 comes in an 8-pin SO or µMAX package, and the MAX978 comes in a 16-pin QSOP or narrow-SO package. Prices start at $1.70 (1000 up, FOB USA).

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.



13-/12-/10-bit, low-power dual DACs fit QSOP-16

In the MAX5152–MAX5159 series of dual D/A converters, the even-numbered DACs (MAX5152, MAX5154, etc.), operate on a single 5V supply and the odd-numbered ones operate on 3V. All feature 3-wire serial inputs, rail-to-rail voltage outputs, and low quiescent current: 500µA during normal operation and only 2µA during shutdown. (The two DACs in each IC can be shut down simultaneously or individually.)

To maximize dynamic range, the output amplifiers for the 10-bit MAX5158/MAX5159 and 12-bit MAX5154/MAX5155 have offset-adjust capability and a fixed gain of two. The 13-bit MAX5152/MAX5153 and 12-bit MAX5156/MAX5157 provide access to the inverting input of each output amplifier, allowing the user to set a specific gain force/sense connection, and maximum output current. These capabilities are well suited for use in industrial process control and digitally programmable 4–20mA current loops.

Each IC is programmed via a 12MHz, 3-wire serial interface compatible with the SPI™, QSPI™, and Microwire™ synchronous-serial standards. In addition, each device features double-buffered inputs, power-on reset, a CLEAR-input pin that resets all DAC outputs to zero, and a serial-data output for daisy-chaining multiple devices.

MAX5152–MAX5159 devices are available in 16-pin DIP and QSOP packages, with prices starting at $4.55 for the 10-bit versions, $6.15 for the 12-bit versions, and $7.95 for the 13-bit versions (1000 up, FOB USA).

SPI and QSPI are trademarks of Motorola, Inc.

Microwire is a trademark of National Semiconductor Corp.

NEW PRODUCTS

Fast differential line receivers deliver 90dB CMR at 10MHz

The MAX4144/MAX4145/MAX4146 triple-op-amp instrumentation amplifiers are intended for use as differential line receivers. With fully symmetrical differential inputs and a single-ended output capable of driving ±3.7V into 150Ω loads, they operate on ±5V, draw 11mA quiescent supply currents, and have a shutdown feature that reduces the supply current to 800µA.

Internal thin-film resistors are matched and laser trimmed to achieve low distortion and common-mode rejection (CMR) as high as 90dB at 10MHz. For the MAX4145, distortion is -92dBc SFDR at f_C = 10kHz. Excellent differential gain/phase and noise specifications make these amplifiers ideal choices for a wide variety of video and RF signal-processing applications. The MAX4144 employs current-feedback techniques to achieve a 130MHz bandwidth and 1000V/µs slew rate. The MAX4145 maintains a 180MHz bandwidth and 600V/µs slew rate at a closed-loop gain of +1V/V, and the MAX4146 maintains a 70MHz bandwidth and 800V/µs slew rate at a closed-loop gain of +10V/V.

To form a complete differential transmission link for digital subscriber lines (DSLs), connect a MAX4144/MAX4145/MAX4146 receiver and MAX4147 differential line driver over a twisted-pair line (see the MAX4147 data sheet for more information). The resulting system replaces multiple high-speed, high-power op amps.

MAX4144/MAX4145/MAX4146 receivers are available in 14-pin SO packages specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $2.40 (1000 up, FOB USA).

Single-supply, gain of +2/-1V/V closed-loop buffers deliver rail-to-rail outputs

The single MAX4214 and MAX4215, dual MAX4217, triple MAX4219, and quad MAX4222 are single-supply buffers that operate with a fixed closed-loop gain of +2V/V or -1V/V, on single supplies of +3.15V to +11V or dual supplies of ±1.575V to ±5.5V. Rail-to-rail outputs and low power consumption make them ideal for portable and battery-powered applications.

Buffers of the MAX4214 family achieve 600V/µs slew rates and ±120mA output-current capability while drawing quiescent supply currents of only 5.5mA. They make an excellent choice for video communications, instrumentation, and other low-power/low-voltage systems that require wide bandwidth. The -3dB bandwidths are 230MHz (MAX4214/MAX4215/MAX4217) and 200MHz (MAX4219/MAX4222). The MAX4215 and MAX4219 have a disable mode, useful in multiplexing applications, that reduces the supply current to 400µA and places the outputs in a high-impedance state.

Inverting and noninverting inputs exhibit the same voltage noise and input-current noise (10nV/√Hz and 1.3pA/√Hz). Other features include 0.1dB gain flatness to 90MHz (MAX4219/MAX4222), low differential gain/phase errors of 0.02%/0.03°, and low distortion at 5MHz: spurious-free dynamic range is -72dBc, and total harmonic distortion is -71dB.

Package options are as follows: a space-saving 5-pin SOT23 (MAX4214), an 8-pin SO or µMAX (MAX4215 and MAX4217), and a 14-pin SOIC or 16-pin QSOP (MAX4219 and MAX4222). All are specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $1.40 (1000 up, FOB USA).

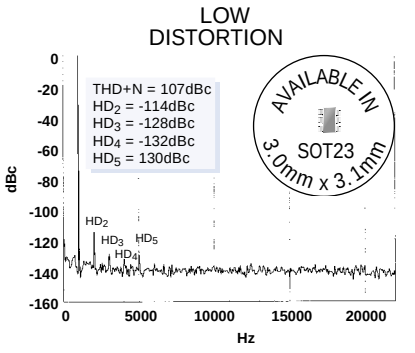
Low-noise, low-distortion amps ideal for portable/battery-powered applications

The MAX4249–MAX4257* series of low-noise, low-distortion amplifiers operate on a single-supply voltage between 5.5V and 2.4V and draw only 400µA of quiescent supply current per amplifier. They make an excellent choice for portable and battery-powered applications that require low noise and/or low distortion. The outputs swing Rail-to-Rail® and the input common-mode range includes ground.

Available as singles, duals, and quads, the MAX4249–MAX4257 op amps outperform their closest available equivalents with respect to input voltage-noise density (7.9nV/√Hz), input current-noise density (0.5fA/√Hz), and ultra-low distortion (0.0002% total harmonic distortion with a 1kΩ load). The MAX4249, MAX4251, MAX4253, and MAX4256 have a low-power shutdown mode that reduces the supply current to 0.5µA and places the outputs in a high-impedance state. The MAX4250–MAX4254 op amps are unity-gain stable. The MAX4249 and MAX4255–MAX4257 devices are internally compensated for gains of 10V/V or greater.

MAX4249–MAX4257 op amps are available in space-saving SOT23-5, µMAX-8, µMAX-10, SO-8, and SO-14 packages. Prices start at $0.83 (1000 up, FOB USA).

**MAX4252/MAX4253/MAX4254 are future products—contact factory for availability.*



NEW PRODUCTS

DAC-controlled boost/inverter LCD-bias supply has internal switch

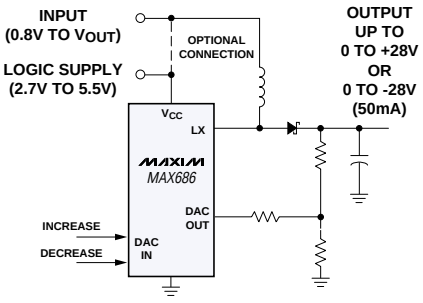
The MAX686 boost/inverter DC-DC converter is designed for LCD-bias generation. It accepts positive inputs in the 2.7V to 5.5V range and produces a regulated output in the 0V to +27V range (or 0V to -27V) as set by an internal 6-bit DAC. The chip also includes programmable current limiting and a 500mA, 28V n-channel MOSFET switch.

MAX686 switching is controlled via current-limited pulse-frequency modulation, which enables high efficiency (to 90%) over a wide range of load conditions. The high switching frequency (to 300kHz) allows use of small external components.

The input and open-drain output of an internal power-OK comparator (POK in, LCDON out) offers protection by providing a signal to disconnect the LCD when its logic voltage is removed. The MAX686 draws about 65µA during normal operation, and only 1.5µA during shutdown. Low power consumption, high efficiency, and a small package make the MAX686 an excellent choice for battery-powered portable equipment.

The MAX686 is similar to the MAX629 with the addition of a DAC. Both devices are supported by evaluation kits that simplify the design process. The MAX686 is available in a 16-pin QSOP package (same size as an 8-pin SO) specified for the extended-industrial temperature range (-40°C to +85°C). Prices for the MAX686 start at $2.95 (1000 up, FOB USA).

INTERNAL 28V SWITCH



Precision PWM buck controller is optimized for next-generation notebook CPUs

The low-voltage MAX1637 pulse-width modulation (PWM) controller is a precision step-down device that generates a precisely regulated, ±2% DC-accurate CPU supply voltage for notebook computers. In systems for which the battery voltage exceeds 5.5V, the MAX1637 receives power separately from the battery (typically from the main +5V supply).

Synchronous rectification by an external MOSFET helps the MAX1637 achieve efficiencies as high as 95%. Efficiency is greater than 80% over a load-current range of 1000:1, which extends battery life in the system-suspend and standby modes of operation. Supply current in shutdown is only 1µA. Excellent load-transient response (within five cycles of a 300kHz clock) prevents the formation of output transients otherwise produced by dynamic-clock CPUs. The chip includes powerful 1A gate drivers to ensure fast switching in the external n-channel MOSFETs.

The MAX1637's fixed-frequency PWM reduces noise and RF interference. When its SKIP input is driven low, the internal Idle Mode™ circuitry optimizes efficiency by automatically lowering the switching frequency in response to light load currents (as load current increases, the device returns smoothly to the PWM mode). For overvoltage protection, a crowbar circuit turns on the low-side MOSFET when the feedback signal goes high by more than 7%. A catastrophic-undervoltage detector shuts down the PWM if the output fails to come into regulation within a preset time interval. An internal digital soft-start reduces the input-surge current at start-up.

The MAX1637 accepts inputs in the 3.15V to 5.5V range and generates an output voltage adjustable from 1.1V to 5.5V. A similar, stand-alone device with low-dropout capability (the MAX1636) includes a 5V/25mA linear regulator (off during shutdown, on during standby mode) that provides a gate-drive supply for the low-side external MOSFET.

The MAX1637 is available in a 16-pin QSOP package specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $3.70 (1000 up, FOB USA).

Idle Mode is a trademark of Maxim Integrated Products.

Micropower linear regulators for notebook computers accept inputs to 28V

The MAX1615 and MAX1616 are low-power linear regulators. Useful in all battery-powered systems, they are designed to provide keep-alive power (always on) to the microcontrollers and CMOS RAM in notebook computers and other systems powered by high-voltage batteries. Each device has a wide input-voltage range (4V to 28V), low dropout voltage (350mV max at the maximum 30mA load current), ±2% initial output accuracy, and low shutdown current (1µA max).

Despite a miserly no-load supply current of 8µA max, the MAX1615/MAX1616 have an excellent AC-PSRR and line-transient response. The MAX1615 provides a clean 5V or 3.3V output even when subjected to the fast supply-voltage changes that occur when switching between battery and AC adapter. The MAX1616's output is adjustable between 1.24V and 24V.

Fault protection includes internal foldback current limiting and thermal-shutdown circuitry. MAX1615/MAX1616 devices are available in a tiny, 5-pin SOT23 package whose excellent thermal characteristics tolerate power dissipation as high as 571mW. Prices start at $0.79 (1000 up, FOB USA).

NEW PRODUCTS

Step-up/step-down DC-DC converter fits in tiny QSOP

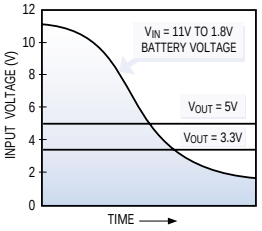
The monolithic MAX1672 combines a low-dropout linear regulator and a high-efficiency, step-up DC-DC converter in a 16-pin QSOP package (same size as an 8-pin SO). It generates a regulated output of 3.3V or 5V for inputs (1.8V to 11V) that vary above and below the output voltage. With two external resistors you can set arbitrary outputs between 1.25V and 5.5V. The typical efficiency in boost mode is 85%.

This step-up/linear-regulator arrangement includes MOSFET pass transistors, and enables the use of a single inductor that is physically smaller than that typically found in a SEPIC or flyback configuration. A digitally selected peak switch-current limit (0.5A or 0.8A) allows use of a still smaller inductor for low-current applications. The linear regulator acts as a filter to reduce the output ripple voltage.

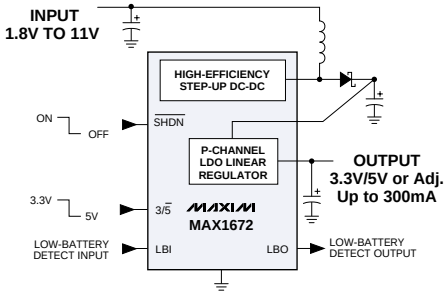
The MAX1672's low quiescent supply current (85µA) is further reduced to 0.1µA during a logic-controlled shutdown. During shutdown, its linear regulator disconnects the output from the input. The device also includes thermal and short-circuit protection and a low-battery detector (PGI/PGO).

A preassembled evaluation kit (MAX1672 EV kit) is available to speed MAX1672 designs. The MAX1672 delivers 300mA at 5V for V_{IN} = 2.5V, and 150mA at 5V for V_{IN} = 1.8V. For a similar but larger device that delivers more output current, look for the MAX710 and MAX711. The MAX1672 is available in a 16-pin QSOP, with prices starting at $2.65 (1000 up, FOB USA).

MAINTAIN CONSTANT OUTPUT OVER VARYING INPUT



300mA STEP-UP/DOWN DC-DC CONVERTER



Switched-capacitor voltage doublers offer 98% efficiency and low power in SOT23

The MAX1682/MAX1683 monolithic-CMOS charge-pump voltage doublers accept inputs between 2V and 5.5V and provide efficiencies exceeding 98%. High efficiency, low operating current (110µA for the MAX1682), and a tiny SOT23-5 package make them ideal for battery-powered and board-level applications. As a typical application, either device operating from 3V can generate 6V for the LCD in a hand-held personal digital assistant (PDA).

The MAX1682 operates at 12kHz and the MAX1683 operates at 35kHz. Both contain oscillator-control circuitry and four power-MOSFET switches. They require only two external capacitors (as low as 1µF), deliver up to 45mA of output current, and exhibit typical output drops of only 600mV at 30mA.

MAX1682/MAX1683 doublers are available in 5-pin SOT23 packages specified for the extended-temperature range (-40°C to +85°C). Prices start at $1.30 (2500 up, FOB USA).

High-accuracy step-down controller powers high-end CPUs

The MAX1638 is a step-down DC-DC controller for generating CPU power in high-end computer systems. Designed for applications in which output voltage precision and good transient response are critical, it generates a regulated output of 1.3V to 3.5V with ±1% total line and load accuracy, and delivers over 35A from an input supply of 5V ±10%. Applications include Intel Pentium Pro®, Pentium II®, PowerPC™, Alpha™, and K6™ systems.

Switching frequency is pin-selectable at 300kHz, 600kHz, or 1MHz. High frequencies reduce board area and cost by enabling the use of smaller output filter capacitors and a small surface-mount inductor.

Excellent dynamic response by the MAX1638 prevents output transients that can otherwise occur in power-supply outputs loaded by the latest dynamically clocked CPUs. Internal flying-capacitor bootstrap circuitry helps provide 2A outputs, which enable the MAX1638 to drive inexpensive n-channel MOSFETs for the external power switch and synchronous rectifier. Synchronous rectification lets the MAX1638 achieve efficiencies greater than 90%.

Other features include a digitally programmable output voltage, an adjustable transient response, selectable AC load regulation (0.5%, 1%, or 2%), internal digital soft-start, power-good output, crowbar overvoltage protection, and a reference output of 3.5V ±1%. A GlitchCatcher™ current-boost circuit, which temporarily bypasses the inductor and its filtering effect, prevents the output spikes caused by fast load changes. Digital inputs D0–D4 are compatible with the Intel VRM 8.2 specification.

The MAX1638 is now available in a 24-pin SSOP, with a 24-pin QSOP scheduled for the future. Prices start at $3.85 (1000 up, FOB USA).

GlitchCatcher is a trademark of Maxim Integrated Products.

Pentium Pro and Pentium II are registered trademarks of Intel Corp.

PowerPC is a trademark of IBM Corp.

Alpha is a trademark of DEC/Compaq.

K6 is a trademark of AMD.

NEW PRODUCTS

Digitally controlled fuel-gauge interface has ±1% absolute accuracy

The MAX1660 fuel-gauge interface provides the fuel-gauging and protection necessary for managing rechargeable battery packs. Operating with a host microcontroller, the MAX1660 accurately monitors charge and discharge currents by storing the accumulated "coulomb counts" in two independent internal counters. It can handle any desired control algorithm and battery chemistry.

The counter contents are made accessible to the controller via a 2-wire serial interface compliant with the System Management Bus (SMBus™). An optional third wire interrupts the controller when the battery charge reaches a programmed capacity limit, or when the instantaneous battery current reaches its limit (also programmed). If an overcurrent or short-circuit condition occurs, the MAX1660 disconnects the load and alerts the controller.

To minimize the part count in a system, the MAX1660 includes a 2.0V precision reference that supplies as much as 200µA to a load, and a 3.3V linear regulator that supplies as much as 5mA for an external controller and other circuitry. A third output provides reliable power-on resets to the external controller. The MAX1660 operates with battery voltages from 4V to 28V, and extends battery life with two micropower shutdown modes: a 1µA hard shutdown, and an 18µA soft shutdown in which the serial interface and 3.3V regulator remain active.

Input current ranges can exceed 24,000:1, and the MAX1660's accuracy is excellent for current ranges exceeding 240:1. For example, the recommended value of current-sense resistor (30mΩ) provides ±1% absolute accuracy over the 17mA to 4A range. The MAX1660 is available in a 16-pin QSOP specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $2.95 (1000 up, FOB USA).

SMBus is a trademark of Intel Corp.

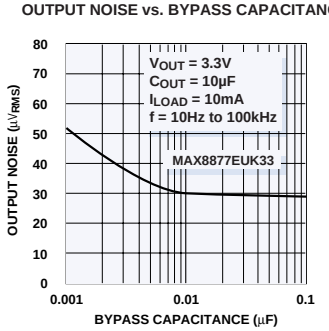
Low-dropout linear regulators feature low 30µV_{RMS} noise

The MAX8867/MAX8868 linear regulators offer an excellent combination of low noise (30µV_{RMS}, 10Hz to 100kHz), low dropout voltage (165mV at the maximum load current of 150mA), and tiny size (SOT23-5 package). This performance enables cell phones and other wireless communications systems to power baseband analog and synthesizer/VCO sections while providing an improved signal-to-noise ratio and longer battery life.

Each device includes a p-channel MOSFET pass transistor that maintains low dropout voltage and a low supply current (100µA) for load currents to 150mA. (The pnp-transistor regulators can draw several milliamps at full load.) To further conserve power, a logic-controlled shutdown reduces the supply current below 1µA. During shutdown, the MAX8868 activates an auto-discharge function that actively discharges the output capacitor to ground.

The standard versions of each regulator are distinguished by common values of pre-set output voltage: 2.5V, 2.8V, 3.0V, 3.15V, 3.3V, 3.6V, and 5.0V. Custom output levels are also available, in 100mV increments from 2.5V to 5.0V. All outputs are specified accurate to ±1.4%. Other features include protection against short circuits, high temperature (thermal shutdown), and reversed-polarity battery connections.

MAX8867/MAX8868 regulators are available in 5-pin SOT23 packages specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $0.88 (2500 up, FOB USA).

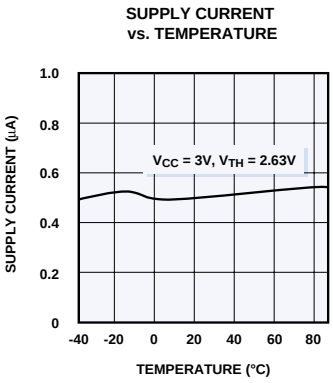


SOT reset ICs draw only 500nA

The MAX6326–MAX6328 ultra-low-power reset circuits are designed to monitor 3V and 3.3V power supplies in digital systems. Ultra-low supply currents (500nA typical) make them ideal for use in portable equipment. By eliminating external components and adjustments, they provide excellent reliability and low cost.

Each device asserts a reset signal of 100ms minimum whenever V_{CC} declines below a preset threshold, and maintains the reset for at least 100ms after V_{CC} returns above that threshold. The ICs differ only in their output structures: active/low push/pull (MAX6326), active/high push/pull (MAX6327), and active/low open-drain (MAX6328). All outputs are guaranteed valid for V_{CC} levels down to 1V. The internal comparator is designed to ignore fast transients on V_{CC}.

The MAX6326–MAX6328 devices will be available with reset threshold voltages in the 2.20V to 3.08V range, in approximate 100mV increments. Five standard thresholds are common to each device (2.20V, 2.32V, 2.63V, 2.93V, and 3.08V), resulting in 15 standard products with a minimum order quantity of 2500 pieces. For nonstandard reset thresholds, please consult the factory. (Minimum nonstandard order quantities are 10k pieces.) MAX6326–MAX6328 devices are available in 3-pin SOT23 packages specified for the extended temperature range (-40°C to +85°C). Prices start at $0.99 (2500 up, FOB USA).



NEW PRODUCTS

Low-noise, 2.5GHz downconverter mixer occupies 10-pin µMAX

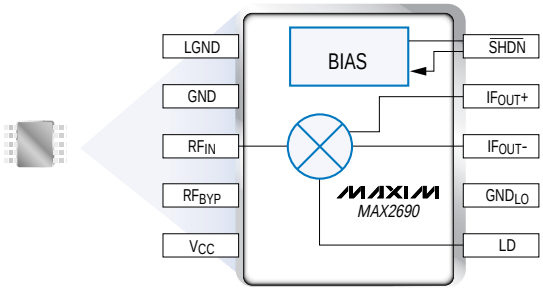
The MAX2690 is a low-noise, low-power downconverter mixer designed for portable consumer equipment. Applications include 2.45GHz industrial-scientific-medical (ISM) radios, wireless LANs, personal communications systems (PCS), code-division multiple-access (CDMA) systems, cellular and cordless phones, and hand-held radios. Its low noise figure (10dB) and high output third-order intercept (OIP3, 15dBm) produce a given RF gain and system sensitivity at much lower levels of supply current.

The single-ended RF input port accepts signals in the 400MHz to 2500MHz range, and the single-ended LO (local oscillator) input port accepts signals in the 700MHz to 2500MHz range. These signals are combined in a double-balanced Gilbert-cell mixer to produce a differential IF output in the range 10MHz to 500MHz. The differential output provides good linearity and low LO emissions, and ensures compatibility with CDMA cellular phones and other applications with differential IF filters.

The MAX2690 operates from a single supply of 2.7V to 5.5V and draws 16mA from a 3V supply. For battery-operated equipment, its logic-controlled shutdown lowers the supply current to <1µA. With a 900MHz RF input and 1.1GHz LO input, the MAX2690 exhibits a gain of 7.7dB and an input third-order intercept (IIP3) of 7.6dBm, resulting in an OIP3 of 15dBm.

The MAX2690 is available in a miniature 10-pin µMAX package priced at $2.20 (1000 up, FOB USA).

SUPER-SMALL DOWNCONVERTER HAS 7.6dBm IIP3



Low-cost, 1.7GHz to 2.05GHz down-converter includes low-noise amplifier

The MAX2406 downconverter, designed for use over a wide frequency range, is optimized for communications systems operating in the 1.9GHz range. Applications include PWT/DCT1900, DCT1800/PCS1900, PHS, and DECT. The MAX2406 includes a low-noise amplifier (LNA), a downconverter mixer, and a local-oscillator (LO) buffer in a low-cost plastic surface-mount package.

The LNA at 1.9GHz has a typical noise figure of 2.5dB and an input third-order intercept point (IIP3) of -9.5dB. The converter mixer has a low noise figure of 9dB and an IIP3 of 4.5dBm. For maximum flexibility, the LO and image-frequency filtering are implemented off-chip.

The MAX2406 has a differential IF port that can operate in single-ended mode when the unused side is tied to V_{CC}. The LO buffer can be driven either differentially or in single-ended mode with as little as -16dBm of LO power. Power consumption, only 60mW in operating mode, drops to 1.5µW in shutdown mode.

For transceiver applications, the MAX2411A and MAX2410 offer a transmitter along with a receiver similar to that of the MAX2406. The MAX2406 is available for $2.38 (1000 up, FOB USA), in a 20-pin QSOP specified for the extended-industrial temperature range (-40°C to +85°C).

RS-485/RS-422 transceivers offer software-selectable, half- or full-duplex operation

MAX1481/MAX1484/MAX1485/MAX1486 data transceivers are ideal for low-cost, space-constrained applications requiring a software-selectable, half- or full-duplex, slew-rate limited RS-485/RS-422 interface that also exhibits high speed (12Mbps) and 1/8-unit loads. All these features are integrated in a 10-pin µMAX package that requires only half the board space of an 8-pin SO.

The MAX1485/MAX1486 (software-selectable, half- or full-duplex) replace larger and more expensive alternatives: a 14-pin, full-duplex transceiver configured via hardware jumpers between the transmit and receive lines, or two 8-pin, half-duplex transceivers that require an additional logic gate to implement software selection. The MAX1481 and MAX1484, functionally equivalent to the industry-standard MAX491 and 75180, provide full-duplex RS-422/RS-485 communications in space-constrained applications.

MAX1481/MAX1485 transceivers feature reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free communications to 250kbps. The driver slew rates for MAX1484/MAX1486 transceivers are not limited, enabling 12Mbps operation for those devices. All exhibit a 1/8-unit-load receiver input impedance that allows as many as 256 transceivers on a single bus.

MAX1481/MAX1484/MAX1485/MAX1486 transceivers are available in 10-pin µMAX packages, with prices starting at $1.25 (1000 up, FOB USA).

NEW PRODUCTS

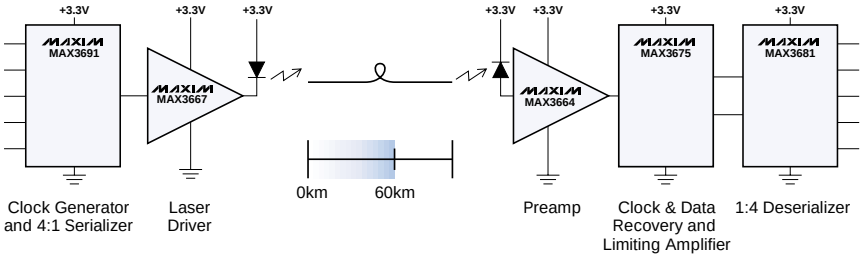
3.3V, 622Mbps laser driver has automatic power control

The MAX3667 is a complete 3.3V (or 5V) laser-diode driver. Designed for SDH/SONET applications operating to 622Mbps, it includes automatic power control (APC) circuitry that compensates for laser-efficiency changes due to temperature effects and aging.

The MAX3667 accepts differential PECL inputs and provides single-ended bias and modulation currents for the laser diode. An internal, temperature-stabilized reference voltage simplifies the external programming of these currents, providing a range of 5mAp-p to 60mAp-p for the modulation current and a range of 5mA to 90mA for the bias current.

To aid external circuitry in supervising the performance of the laser-driver system, two internal monitors provide high-speed analog currents that are directly proportional to the bias and modulation currents. Other features include enable/disable control and a slow-start capability with 50ns minimum turn-on time. The MAX3667 is available in a 32-pin TQPF package specified for the extended-industrial temperature range (-40°C to +85°C). Prices start at $9.95 (1000 up, FOB USA).

COMPLETE 3.3V TRANSMITTER/RECEIVER CHIPSET INCLUDES CLOCK GENERATOR AND SERIALIZER



622Mbps LAN/ATM laser driver has programmable modulation current

The MAX3766 laser driver is designed for fiber optic LAN transmitters and optimized for operation at 622Mbps. It includes a laser modulator, automatic power control (APC) circuitry, and a fail indicator with latched shutdown.

An external resistor programs the laser's modulation current (the maximum at 622Mbps is 60mA). Another resistor programs the laser's bias current between 0.5mA and 80mA. At lower modulation currents, the MAX3766 can operate at data rates to 1.25Gbps. The temperature coefficient of modulation can also be programmed to keep the transmitter extinction ratio nearly constant over a wide temperature range. APC circuitry, using feedback from the laser's monitor photodiode, adjusts the laser's bias current to produce a constant output power regardless of the laser's temperature or age.

To ensure that the transmitter output does not reach hazardous levels, the MAX3766 provides extensive laser-safety measures including a failure indicator with latched shutdown and a smooth-startup bias generator. The MAX3766 is available in a 20-pin QSOP package priced at $12.17 (1000 up, FOB USA).

5-tap silicon delay lines cover the 4ns to 500ns range

The MXD1000/MXD1005 silicon delay lines each have five taps, offering five delay values arranged in 20% increments of the maximum delay available. This maximum depends on the product version, as indicated by a part-number extension in nanoseconds. The MXD1000 comes in 8 versions; the MXD1005 in 16. Each tap drives as many as ten 74LS loads.

The MXD1000 and MXD1005 operate on 5V and have TTL/CMOS-compatible digital inputs. Each delay value has a nominal accuracy of ±2ns or ±3%, whichever is greater. When compared with hybrid delay lines, these offer better performance, higher reliability, and lower cost. MXD1000/MXD1005 devices are improved second sources for the DS1000/DS1005 from Dallas Semiconductor. MXD1000 supply current is 20mA (vs. 35mA for the DS1000), and MXD1005 supply current is 17mA (vs. 40mA for the DS1005).

The MXD1000 and MXD1005 are available in an 8-pin DIP, SO, or µMAX package, a 14-pin DIP package, and a 16-pin narrow-SO package. Prices start at $1.82 (MXD1000) and $2.28 (MXD1005) (1000 up, FOB USA).

ACTIVE CURRENT vs. FREQUENCY (MXD1000__075 vs. DS1000-75)